FIG. 1

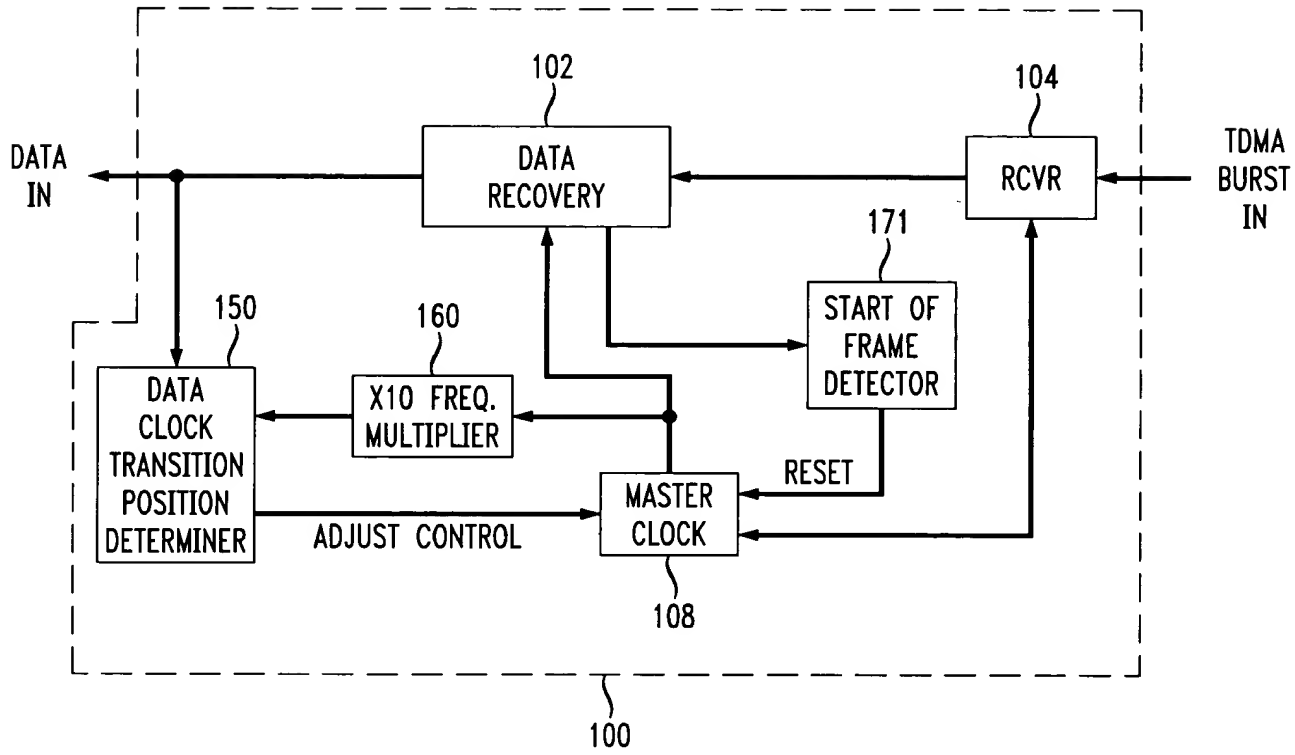

102
104
DATA IN
DATA RECOVERY
RCVR
TDMA BURST IN
171
START OF FRAME DETECTOR
150
160
DATA CLOCK TRANSITION POSITION DETERMINER
X10 FREQ. MULTIPLIER
RESET
MASTER CLOCK
ADJUST CONTROL
108
100

FIG. 1A 2/9

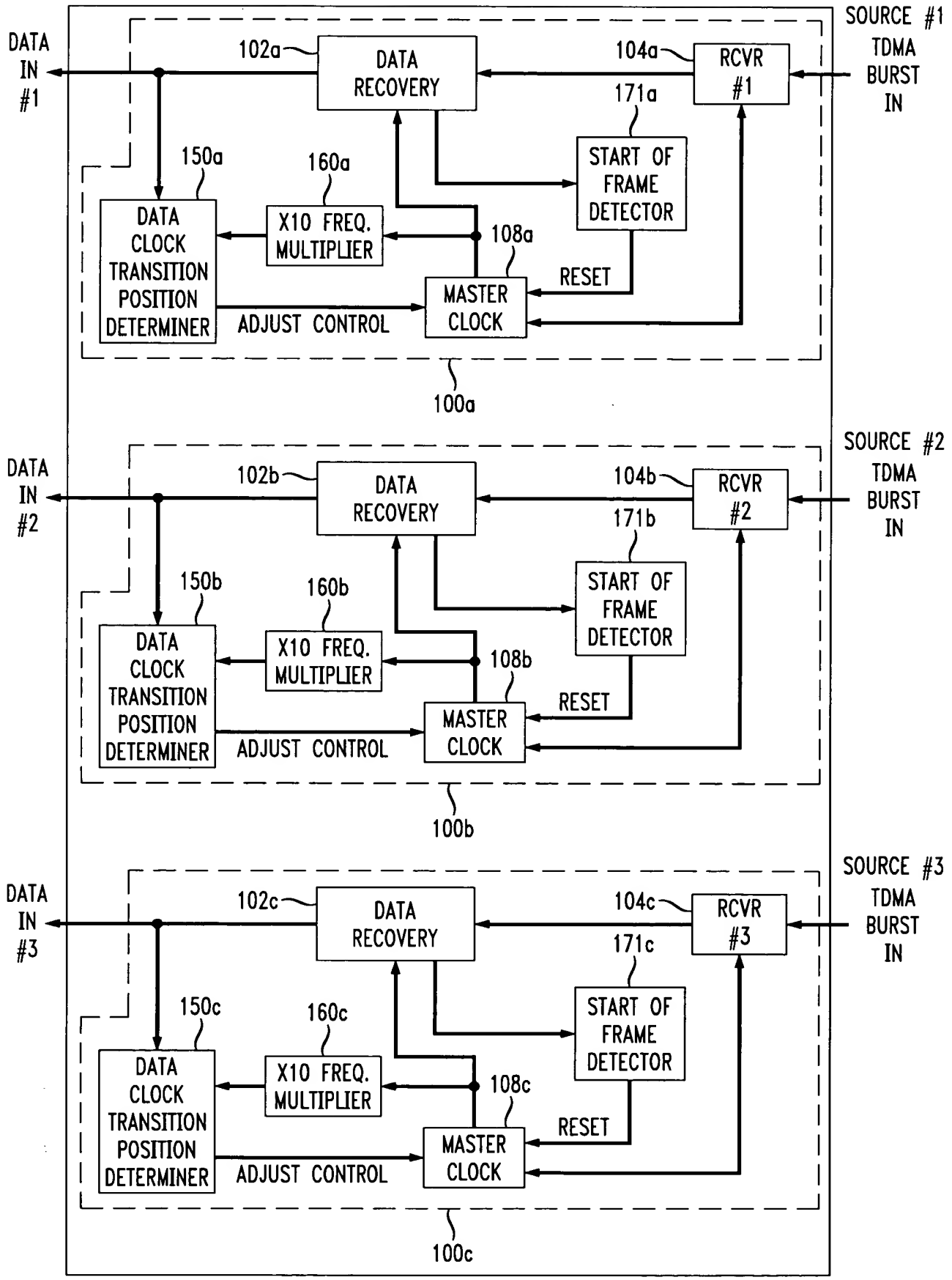
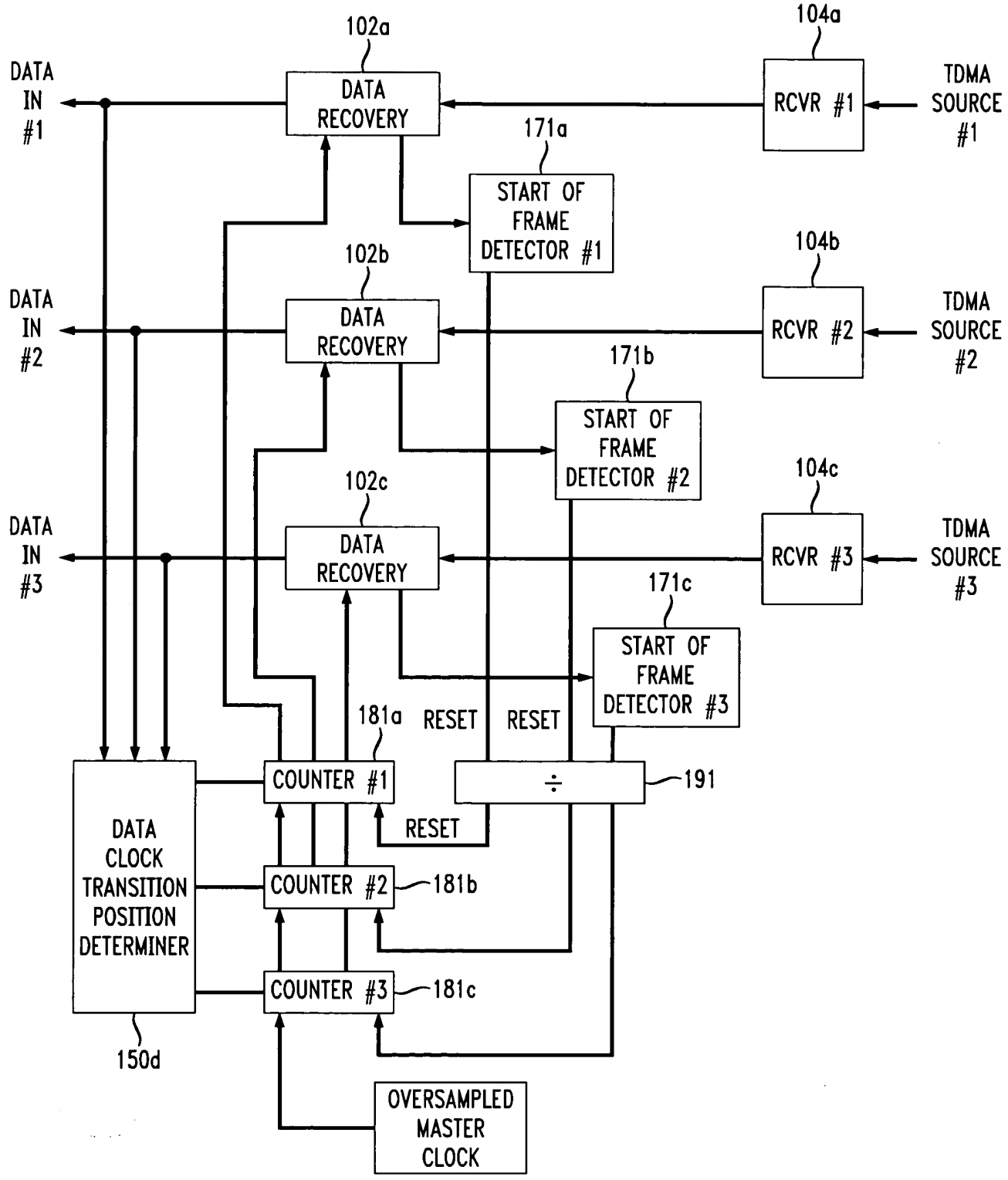

DATA IN #1
102a
DATA RECOVERY
104a
RCVR #1
SOURCE #1 TDMA BURST IN
171a
START OF FRAME DETECTOR
150a
160a
DATA CLOCK TRANSITION POSITION DETERMINER
X10 FREQ. MULTIPLIER
108a
RESET
MASTER CLOCK
ADJUST CONTROL
100a
DATA IN #2
102b
DATA RECOVERY
104b
RCVR #2
SOURCE #2 TDMA BURST IN
171b
START OF FRAME DETECTOR
150b
160b
DATA CLOCK TRANSITION POSITION DETERMINER
X10 FREQ. MULTIPLIER
108b
RESET
MASTER CLOCK
ADJUST CONTROL
100b
DATA IN #3
102c
DATA RECOVERY
104c
RCVR #3
SOURCE #3 TDMA BURST IN
171c
START OF FRAME DETECTOR
150c
160c
DATA CLOCK TRANSITION POSITION DETERMINER
X10 FREQ. MULTIPLIER
108c
RESET
MASTER CLOCK
ADJUST CONTROL
100c

FIG. 1B


DATA IN #1
DATA IN #2
DATA IN #3
102a
102b
102c
DATA RECOVERY
DATA RECOVERY
DATA RECOVERY
104a
104b
104c
RCVR #1
RCVR #2
RCVR #3
TDMA SOURCE #1
TDMA SOURCE #2
TDMA SOURCE #3
171a
171b
171c
START OF FRAME DETECTOR #1
START OF FRAME DETECTOR #2
START OF FRAME DETECTOR #3
181a
RESET
RESET
COUNTER #1
÷
191
RESET
DATA CLOCK TRANSITION POSITION DETERMINER
COUNTER #2
181b
COUNTER #3
181c
150d
OVERSAMPLED MASTER CLOCK

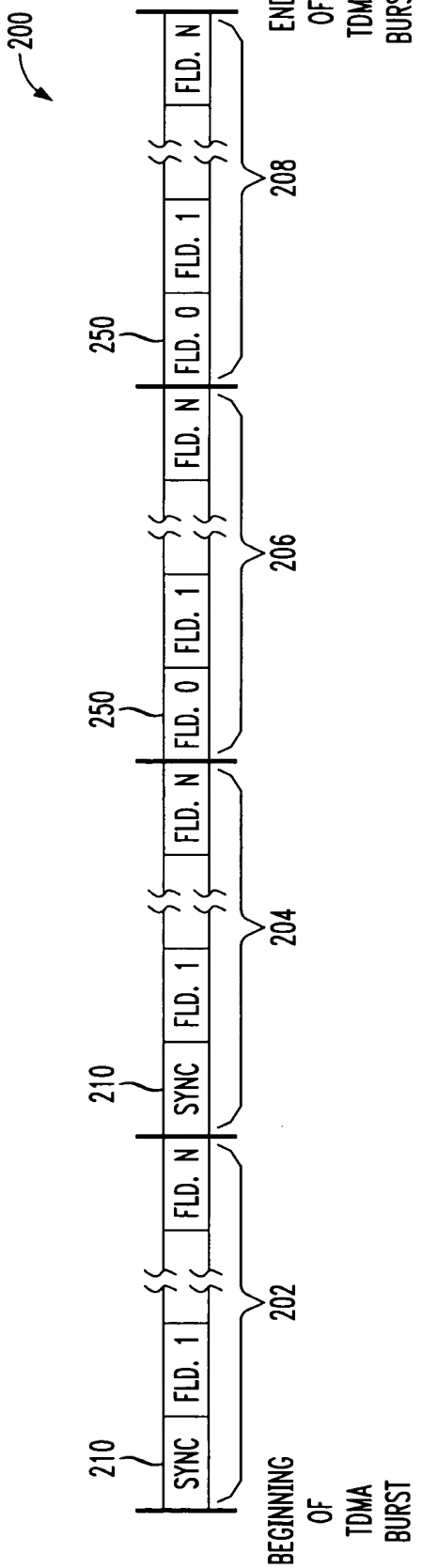

200
SYNC
FLD. 1
FLD. N
FLD. 0
FLD. 1
FLD. N
210
250
202
204
206
208
BEGINNING OF TDMA BURST
END OF TDMA BURST

FIG. 2

FIG. 3A

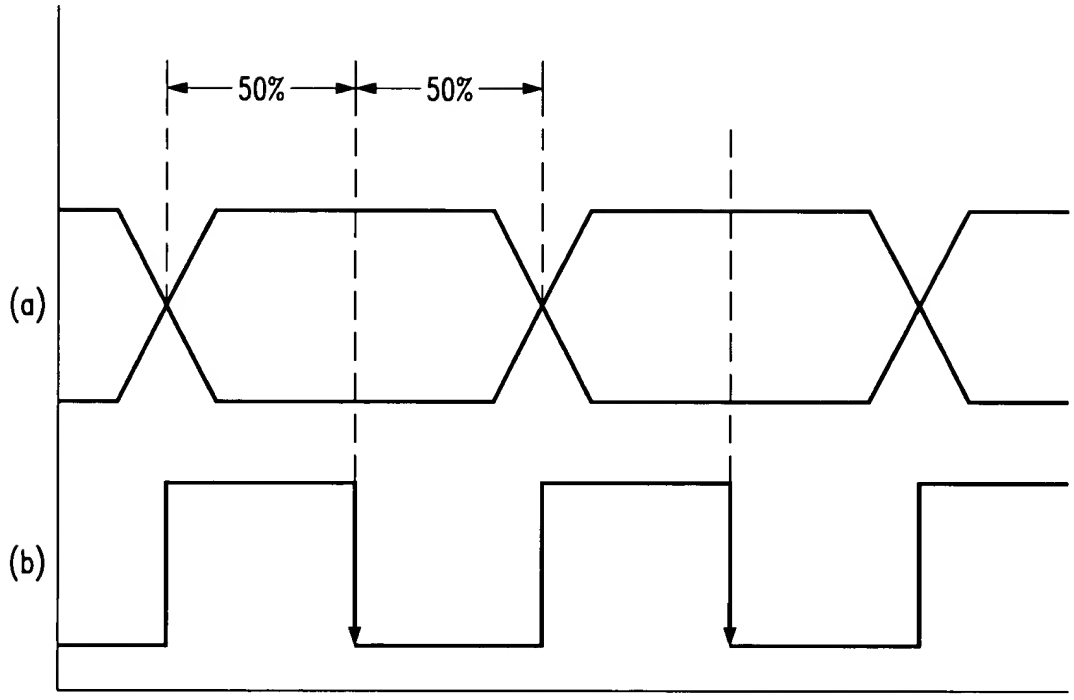
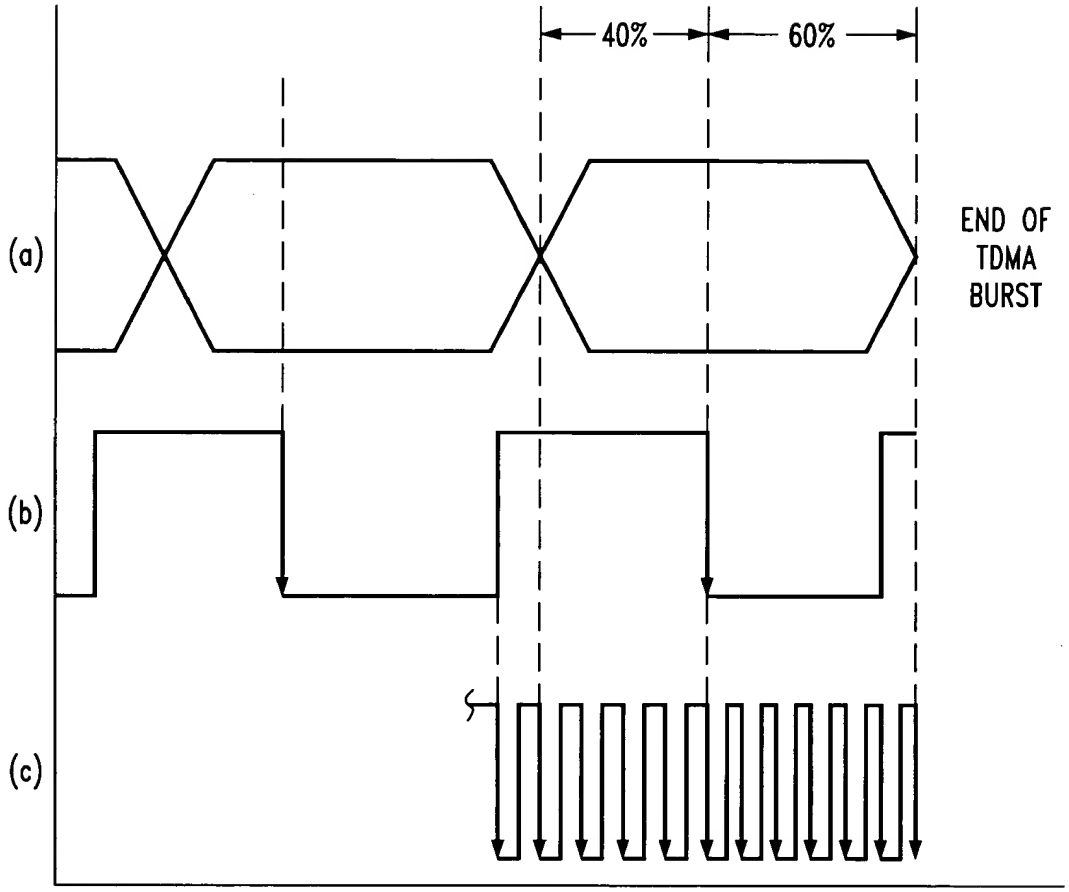


FIG. 3B



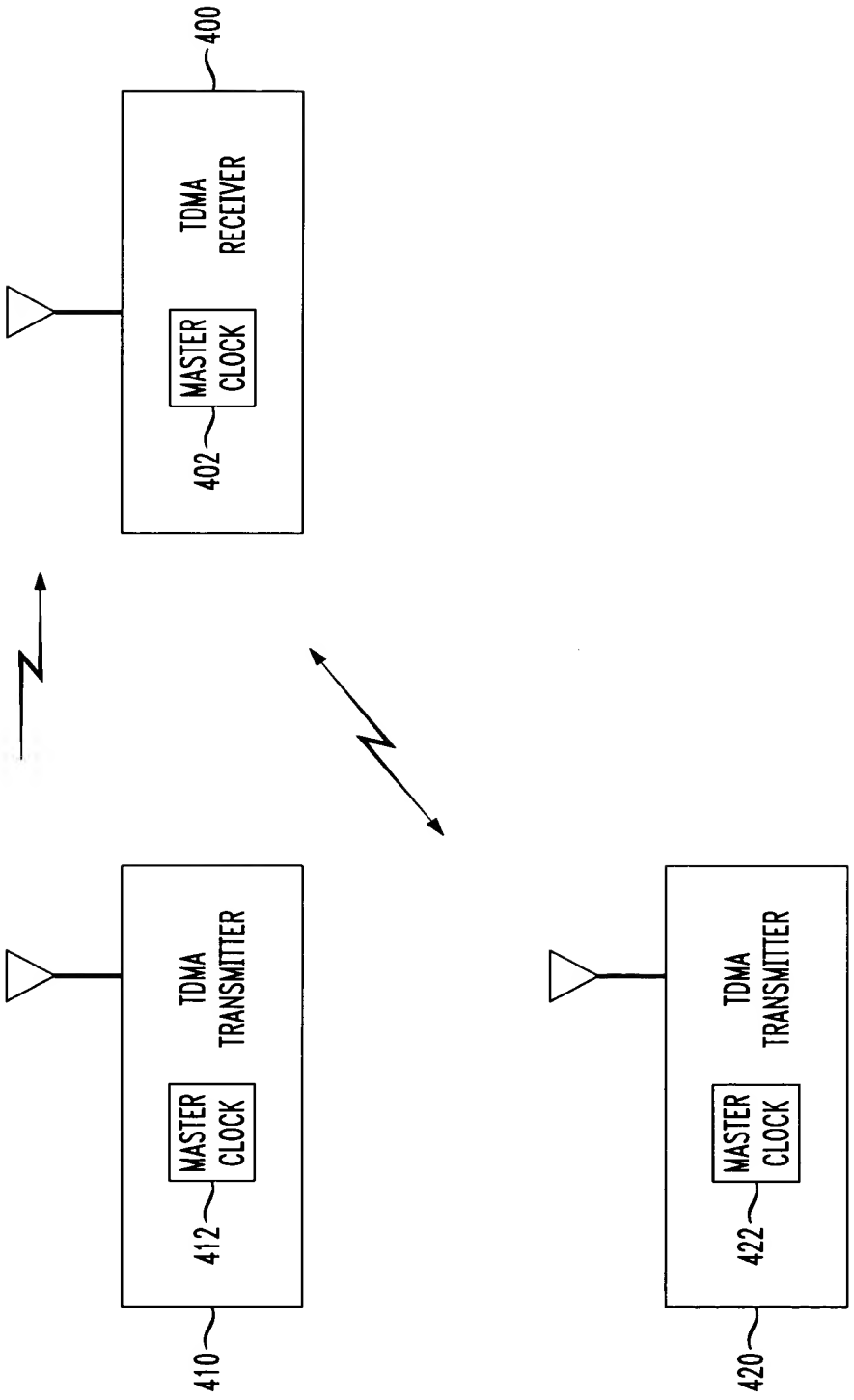
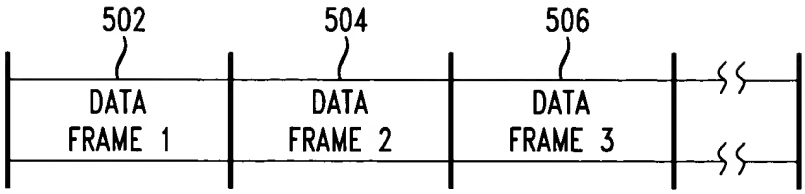


FIG. 4
PRIOR ART

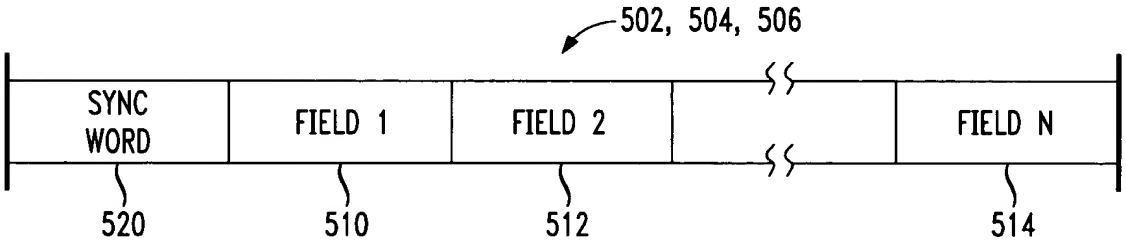
FIG. 5A



TDMA BURST

FIG. 5B

PRIOR ART



DATA FRAME

FIG. 6
PRIOR ART

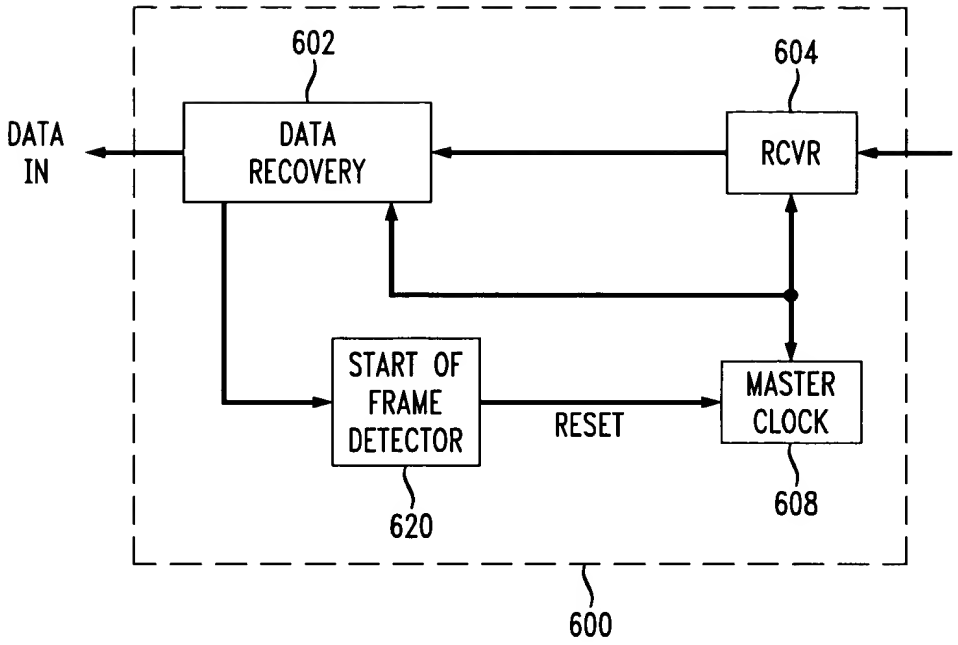
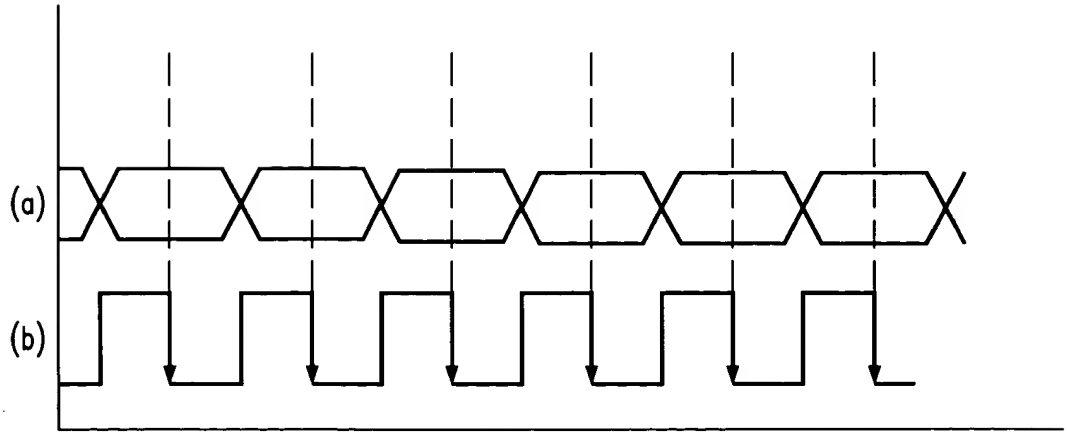



FIG. 7
PRIOR ART